

Remarks

Applicant appreciates the Examiner's indicating allowable subject matter in claims 5, 9 and 11.

Applicant cancelled claim 5 and added its subject matter to claim 1. Applicant deleted the word "layer," and the subject matter "by blanket epitaxy" from claim 1.

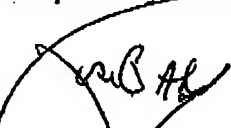
Applicant added new dependent claim 23, which re-presents the subject matter deleted from claim 1.

Accordingly, Applicant believes that any rejection under 35USC112 is overcome, and that claims 1-4, 6-11 and claim 23 are allowable.

Neither Taka et al., nor Chen et al., applied either singly or in combination, teaches, discloses or suggests "the semiconductor intrinsic base layer includes silicon germanium."

Entry and allowance of claims 1-4, 6-11, 23 are solicited.

Respectfully submitted,

 10-29-03  
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**WHAT IS CLAIMED IS:**

1           1. (Currently Amended) A bipolar transistor, comprising:

2                   a substrate;

3                   a semiconductor intrinsic base layer formed by ~~blanket epitaxy~~ on the substrate;

4                   a collector layer formed on the substrate, wherein the semiconductor intrinsic base  
5 layer includes silicon germanium;

6                   an emitter formed over the semiconductor intrinsic base layer, forming a junction  
7 between the semiconductor intrinsic base layer and the emitter, wherein the junction at a lateral  
8 portion of the emitter extends farther into the intrinsic base layer than the junction at a center  
9 portion of the emitter;

10                  an extrinsic base formed adjacent to the lateral portion of the emitter;

11                  a base electrode formed on a portion of the extrinsic base layer;

12                  a collector electrode formed on a portion of the collector layer; and

13                  an emitter electrode formed on a portion of the emitter-layer.

14  
15           2. (Currently Amended) ~~A~~ The bipolar transistor as claimed in claim 1, wherein the  
16 emitter comprises a pedestal having a top which contacts an emitter layer.

17  
18           3. (Currently Amended) ~~A~~ The bipolar transistor as claimed in claim 1, wherein a raised  
19 extrinsic base layer is formed and comprises one of a highly-doped polysilicon or a highly-doped  
20 amorphous silicon.

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1  
2 4. (Currently Amended) A The transistor as ~~recited~~ claimed in claim 1, wherein the  
3 lateral portion has a depth in a range of approximately 20-40 nm.

4  
5 5. (Cancelled)

6  
7 6. (Currently Amended) A The bipolar transistor as ~~recited~~ claimed in claim 1, further  
8 comprising a sidewall spacer formed between and electrically isolating the emitter and the  
9 extrinsic base layer.

10  
11 7. (Currently Amended) A The bipolar transistor as ~~recited~~ claimed in claim 6, wherein  
12 the sidewall spacer comprises one of a silicon nitride, a silicon dioxide, or a combination of the  
13 two.

14  
15 8. (Currently Amended) A The bipolar transistor as ~~recited~~ claimed in claim 7, wherein  
16 the sidewall spacer has a width in the range of 10 to 70 nanometers.

17  
18 9. (Currently Amended) A The bipolar transistor as ~~recited~~ claimed in claim 2, wherein  
19 the emitter comprises one of a polysilicon or an amorphous silicon.

20  
21 10. (Currently Amended) A The bipolar transistor as ~~recited~~ claimed in claim 1, wherein  
22 the emitter layer has a thickness in the range of 30 to 200 nanometers.

23  
  
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24 11. (Currently Amended) A The bipolar transistor as recited ~~claimed~~ in claim 1, wherein  
25 the emitter is in-situ doped with phosphorous that minimizes drive-in and activation anneal  
26 temperatures.

27

28 Claims 12 -22 (Withdrawn)

29

30 23. (New) The transistor as claimed in claim 1, wherein the semiconductor intrinsic base  
31 layer is formed by blanket epitaxy.

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